--

GOVERNMENT RIGHTS

This invention was made with government support under Grant No. N00014-92-J-1519 awarded by the Department of Navy Research. The government has certain rights in the invention.

REFERENCE TO RELATED APPLICATIONS

This is a continuation of U.S. Patent Application Serial No. 09/020,565 filed January 16, 1998, now pending, which is a continuation of international application No. PCT/US97/00629 filed January 16, 1997 which designated the United States, now abandoned, which is a continuation-in-part of U.S. Patent Application Serial No. 08/587, 411 filed January 16, 1996, now issued as U.S. Patent No. 5,872,387. --

IN THE CLAIMS:

Please cancel claims 15-27 and 36-39, all claims presently pending. Please enter the following new claims:

-- 40. (New) A field effect transistor having an interface between a semiconductive silicon layer and a gate oxide layer, characterized by post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature of at least about 200°C so as to increase the resilience of the field effect transistor to hot electron effects, said post-fabrication passivation being conducted

sufficiently to provide to said transistor a practical lifetime at least about ten times that provided by a corresponding passivation with hydrogen, wherein practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.

41. (New) The field effect transistor of claim 40 wherein said gate oxide layer comprises silicon dioxide.

42. (New) The field effect transistor of claim 40, wherein said semiconductive silicon layer is a crystalline silicon layer.

43. (New) The field effect transistor of claim 41, which is an insulated gate field effect transistor, and wherein said post-fabrication passivation is conducted for a period of at least about one hour.

44. (New) The field effect transistor of claim 43, wherein said semiconductive silicon layer is a crystalline silicon layer.

45. (New) The field effect transistor of claim 44, wherein said deuterium gas-enriched atmosphere contains from about 0.1% to 100% by volume deuterium gas.

46. (New) The field effect transistor of claim 40, comprising deuterium atoms from said post-fabrication passivation covalently bonded at said interface.

47. (New) The field effect transistor of claim 40, which is encapsulated.

48. (New) The field effect transistor of claim 40, which comprises a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate oxide layer over said channel, said interface between said gate oxide layer and said channel, and conductive contacts for said drain, said source and said gate oxide; and

wherein said post-fabrication passivation provides covalently-bound deuterium populating said interface.

49. (New) A passivated field effect transistor obtained by:

providing a field effect transistor comprising a semiconductive silicon layer, a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between said drain and said source, a gate oxide layer over said channel, an interface between said gate oxide layer and said channel, and conductive contacts for said drain, source and gate oxide; and

subjecting said field effect transistor to a heated, deuterium gas-enriched ambient so as to cause deuterium atoms from said deuterium gas to be covalently bound in the area of said interface and thereby increase the resilience of said field effect transistor to hot electron effects caused by channel electrons entering the gate oxide.

50. (New) The device of claim 49, wherein said gate oxide layer comprises an oxide of silicon.

51. (New) The device of claim 49, wherein said gate oxide layer comprises silicon dioxide.

52. (New) The device of claim 49, which is encapsulated.

53. (New) The device of claim 52, which comprises a plurality of insulated gate field effect transistors.